

| ISSUE CLASSIFICATION | |
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| Class | Subclass |
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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

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| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
| 09/773595 | F | 713 | | 2182 | <i>ee Du</i> |

APPLICANTS

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Yasuhiko Hagihera

TIME

Delay adjustment circuit and a clock generating circuit using the same

PTO-2040
12/99

ISSUING CLASSIFICATION

| ORIGINAL | | | | CROSS REFERENCE(S) | | | |
|------------------------------|--|----------|--|--------------------|--|-----------------------------------|--|
| CLASS | | SUBCLASS | | CLASS | | SUBCLASS (ONE SUBCLASS PER BLOCK) | |
| INTERNATIONAL CLASSIFICATION | | | | | | | |
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|--|---|-------------|------------|-----------------------------------|----------------------|
| TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
| | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| <input checked="" type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. | _____ (Assistant Examiner) _____ (Date) | | | NOTICE OF ALLOWANCE MAILED | |
| <input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ | | | | ISSUE FEE | |
| _____ | | | | Amount Due | Date Paid |
| <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed. | _____ (Primary Examiner) _____ (Date) | | | ISSUE BATCH NUMBER | |
| _____ (Legal Instruments Examiner) _____ (Date) | | | | | |

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